Anirudh Mohan Kaushik

Unit 905, 17 Barrel Yards Blvd., Waterloo, Ontario, Canada N2L0E4

anirudh.m.kaushik@protonmail.com

Personal Information

- Birth: May 31, 1990, Muscat, Sultanate of Oman
- Current Address: Unit 905, 17 Barrel Yards Blvd., Waterloo, Ontario, Canada N2L0E4
- Country of Citizenship: Canada

Current Position

- **Intel Canada** — **Toronto, Canada**
  Software Development Engineer — *December 2021*
  Member of Intel Graphics Compiler (IGC) team. Responsible for research and design of compiler back-end, feature development, and code optimizations for compute and graphics workloads.

Education

- **Doctor of Philosophy (PhD), Computer Engineering** — **Waterloo, Canada**
  University of Waterloo — *2015–2021*
  Advisor: Professor Hiren Patel
  Ontario Graduate Scholarship (2017, 2018, 2019)
  President's Graduate Scholarship (2017, 2018, 2019)
  University of Waterloo Graduate Scholarship (Spring 2017, Fall 2018)

- **Master of Applied Sciences (MASc), Computer Engineering** — **Waterloo, Canada**
  University of Waterloo — *2012–2014*
  Advisor: Professor Hiren Patel
  Thesis: Accelerating Mixed-Abstraction SystemC Models on Multi-Core CPUs and GPUs
  University of Waterloo Graduate Scholarship (Winter 2014)

- **Bachelor of Technology (BTech), Electronics and Communications** — **Vellore, India**
  Vellor Institute of Technology University, GPA: 82/100 — *2008–2012*
  Thesis: Efficient multi-ported memories for FPGAs

Previous Employment

- **Advanced Micro Devices (AMD)** — **Austin,Texas, USA**
  Member of Technical Staff — *March 2021–December 2021*
  Member of Data Fabric Team. Data fabric is the main interconnect IP across all AMD chip offerings. Responsible for post-silicon feature enablement and support performance, functional, and power investigations related to data fabric.

- **Advanced Micro Devices (AMD) Research** — **Austin, Texas, USA**
  Research intern with Compute on Graphics (COG) team — *October 2018–April 2019*
- **International Business Machines (IBM)** — **Markham, Canada**
  Software performance analyst (Intern) with POWER performance team — *May 2014–August 2015*

Patents

- Hardware assisted fine-grained data movement
  United States Patent US11734059B2
  Application filed in 2019, Granted in 2023
  (Patent from work at AMD Research)

Publications

Conference publications

- Predictable GPU Wavefront Splitting for Safety-Critical Systems
  Artem Klashtorny, Zhuanhao Wu, Anirudh M Kaushik, and Hiren Patel
  In ACM/IEEE International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), 2023

- ZeroCost-LLC: Shared LLCs at No Cost to WCL
  Zhuanhao Wu, Anirudh M Kaushik, and Hiren Patel
  In IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2023

- Automated Synthesis of Predictable and High-Performance Cache Coherence Protocols
  Anirudh M Kaushik, and Hiren Patel
  In IEEE Conference on Design Automation and Test in Europe (DATE), 2021

- A Systematic Approach to Achieving Tight Worst-Case Latency and High-Performance Under Predictable Cache Coherence
  Anirudh M Kaushik, and Hiren Patel
  In IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2021

- A Hardware Platform for Exploring Predictable Cache Coherence Protocols for Real-time Multi-cores
  Zhuanhao Wu, Anirudh M Kaushik, Paulos Tegegn, and Hiren Patel
  In IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2021

- Optimizing Hyperplane Sweep Operations using Asynchronous Multi-grain GPU Tasks
  Anirudh M. Kaushik, Ashwin M. Aji, Muhammad Amber Hassaan, Noel Chalmers, Noah Wolfe, Scott Moe, Bradford M. Beckmann, and Sooraj Puthoor
  In IEEE International Symposium on Workload Characterization (IISWC), 2019

- CARP: A Data Communication Mechanism for Multi-Core Mixed-Criticality Systems
  Anirudh M Kaushik, Paulos Tegegn, Zhuanhao Wu, and Hiren Patel
  In IEEE Real-Time Systems Symposium (RTSS), 2019

- Enabling Predictable, Simultaneous and Coherent Data Sharing in Mixed Criticality Systems
  Nivedita Sritharan, Anirudh M Kaushik, Mohamed Hassan and Hiren Patel
  In IEEE Real-Time Systems Symposium (RTSS), 2019

- Predictable cache coherence for multi-core real-time systems
  Mohamed Hassan, Anirudh M Kaushik, and Hiren Patel
  In IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2017

- Reverse-engineering embedded memory controllers through latency-based analysis
  Mohamed Hassan, Anirudh M Kaushik, and Hiren Patel
  In IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2015

- SystemC-clang: An open-source framework for analyzing mixed-abstraction SystemC models
  Anirudh M Kaushik and Hiren D Patel
  In IEEE Forum on Specification & Design Languages (FDL), 2013

- On the use of GP-GPUs for accelerating compute-intensive EDA applications.
  Valeria Bertacco, Debapriya Chatterjee, Nicola Bombieri, Franco Fummi, Sara Vinco, Anirudh M Kaushik, and Hiren D Patel
  In IEEE Conference on Design, Automation and Test in Europe (DATE), 2013

- Accelerating SystemC simulations using GPUs
  Mahesh Nanjundappa, Anirudh M Kaushik, Hiren D Patel, and Sandeep K Shukla
  In IEEE High Level Design Validation and Test Workshop (HLDVT), 2012

Journal publications

- Automatic Construction of Predictable and High-Performance Cache Coherence Protocols for Multi-Core Real-Time Systems
  Anirudh M Kaushik and Hiren Patel
  In IEEE Transactions on Computer Aided Design (TCAD), 2022

- Gretch: A Hardware Prefetcher for Graph Analytics
  Anirudh M Kaushik, Gennady Pekhimenko, and Hiren Patel
  In ACM Transactions on Architecture and Code Optimization (TACO), 2020

- Designing Predictable Cache Coherence Protocols for Multi-Core Real-Time Systems
  Anirudh M Kaushik, Mohamed Hassan, and Hiren Patel
  In IEEE Transactions on Computers (TC), 2020

- Exposing Implementation Details of Embedded DRAM Memory Controllers through Latency-based Analysis
  Mohamed Hassan, Anirudh M Kaushik, and Hiren Patel
  In ACM Transactions on Embedded Computing Systems (TECS), 2018

Presentations

- Automated Synthesis of Predictable and High-Performance Cache Coherence Protocols
  DATE, Virtual, 2021
- A Systematic Approach to Achieving Tight Worst-Case Latency and High-Performance Under Predictable Cache Coherence
  RTAS, Virtual, 2021
- Predictable cache coherence for multi-core real-time systems
  RTAS, Pittsburgh, 2017
- Reverse-engineering embedded memory controllers through latency-based analysis
  RTAS, Seattle, 2015
- SystemC-clang: An open-source framework for analyzing mixed-abstraction SystemC models
  FDL, Paris, 2013

Teaching experience

- Teaching assistant for ECE 222: Digital Computers (Winter 2013, Fall 2016)
- Teaching assistant for ECE 429: Computer Architecture and Organization (Spring 2017, 2018)

Technical and Personal skills

- **Programming Languages:** C, C++, Python, SQL, Unix shell scripting, Verilog, VHDL, SystemC
- **Technologies:** clang for LLVM, Xilinx tool chain for FPGAs, Micro-architectural simulators: Sniper and gem5, PostgreSQL, Git

Volunteering experience

- **LAUNCH Waterloo** **Waterloo, Canada**
  STEAM Intermediate league *September 2023*
  I volunteered as an assistant coach for STEAM intermediate league, LAUNCH Waterloo. STEAM intermediate league consisted of students in grades 4-5 working on STEM related projects. I assisted the head volunteer with setting up activities and assisting students in completing the activities.
- **Girl Day** **Austin, Texas, USA**
  UT Austin *February 2019*
  I volunteered as part of the AMD team, and helped set up and organize the AMD booth at Girl Day. Girl Day is a free event for K-8 students where students get the chance to explore engineering, science, math, and technology at their own pace throughout the event. I participated in helping students build simple electrical circuits and showcase AMD's offerings in virtual and augmented reality.
- **Junior Achievement** **Markham, Canada**
  J.A Titan *July 2015*
  I volunteered as part of the IBM Toronto team, and helped organize Junior Achievement (JA) Titan 3.0. JA Titan 3.0 is a business simulation challenge for high school students to understand the economics of managing a business. As a volunteer, I counseled students on the benefits of investment in different areas and how to maximize business efficiency.
- **Junior Achievement** **Markham, Canada**
  Economics for Success *November 2014*

I volunteered as part of the IBM Toronto team, and conducted a full-day session for Grade 8 students on "Economics for Success". I spoke to students about the importance of staying in school and how to efficiently manage day-to-day finances. Activities included talking about personal experience as a student, conducting games, and counseling students on fulfilling ambitions.

References

- **Professor Hiren Patel**
  Professor
  Electrical and Computer Engineering
  University of Waterloo, Waterloo, Canada
  hiren.patel@uwaterloo.ca

- **Professor Rodolfo Pellizzoni**
  Professor
  Electrical and Computer Engineering
  University of Waterloo, Waterloo, Canada
  rpellizz@uwaterloo.ca

- **Professor Nachiket Kapre**
  Associate Professor
  Electrical and Computer Engineering
  University of Waterloo, Waterloo, Canada
  nachiket@uwaterloo.ca

- **Dr. Bradford Beckmann**
  Principal Member of Technical Staff
  AMD Research
  Bellevue, Washington, USA
  brad.beckmann@amd.com